Scientific Journal of Impact Factor (SJIF): 4.14

e-ISSN (O): 2348-4470
p-ISSN (P): 2348-6406

International Journal of Advance Engineering and Research Development

Volume 3, Issue 11, November -2016

Review on "FPGA based high speed, low power matrix multiplier using Urdva Triyagbhyam algorithm".

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ABSTRACT- *Matrix multiplication is a computation intensive operation and plays an important role in many scientific and engineering applications such as image processing, discrete signal processing. This paper presents architecture for the multiplication of two matrices using Field Programmable Gate Array (FPGA).This paper presents unsigned two 3x3 High-Speed matrix multiplier The hierarchical structuring has been used to optimize for multipliers using "Urdhava Trigyagbhyam" sutra (vertically and crosswise)which is one of the sutra for Vedic mathematics. Each element of matrix is represented by 4-bit,output is of 8 bit. The coding has been done using VHDL and synthesized using Altera Quartus II. A concept of design is hierarchical structuring; This gives less computation time for calculating the multiplication result. We will synthesized the proposed designs and the existing design using Altera Quartus II tools. The proposed structure consumes less energy.*

Key words: *FPGA, Matrix multiplier,vedic, Urdhava Trigyagbhyam ,VHDL*

I. INTRODUCTION

Matrix multiplication is frequently used operation in a wide variety of graphics, image processing, robotics, and signal processing applications. The increases in the density and speed of field-programmable gate arrays (FPGAs) make them attractive as flexible and high-speed alternatives to DSPs and ASICs. It is a highly procedure oriented computation , there is only one way to multiply two matrices and it involves lots of multiplications and additions. But the simple part of matrix multiplication is that the evaluation of elements of the resultant elements can be done independent of the other, this point to distributed memory approach. In this paper, we propose an architecture that is capable of handling matrices of variable sizes Our designs minimize the gate count, area, improvements in latency, computational time, throughput for performing matrix multiplication and reduces the number of multiplication and additions hardware required to get the matrices multiplied on commercially available FPGA devices.Matrix multiplication is a frequently used kernel operation in a wide variety of graphics, image processing, robotics, and signal processing applications. Several signal and image processing operations can be reduced to matrix multiplication. Most of the previous work on matrix multiplication on FPGAs focuses on latency optimization .

However, since mobile devices typically operate under various computational requirements and energy constrained environments, energy is a key performance metric in addition to latency and throughput . Hence, in this paper, we develop designs that minimize the energy dissipation. Our designs offer tradeoffs between energy, area, and latency for performing matrix multiplication. The architecture design in our work to multiply two numbers is use the multiplier unit used for multiplying two numbers in a single clock cycle. This increases the speed of the computation. The proposed architecture realized on FPGA which is based on Vedic Multiplication sutra(algorithm) "Urdhava Trigyagbhyam" .The implementation architecture is also use of IP CORE(Intellectual Property) for adders which allows us to be optimized for speed and space. The objective of this paper is to propose a low area, speed , energy efficient, maximum running frequency, low power, matrix multiplier.

II. LITERATURE REVIEW

A Number of experimental investigations have been reported for matrix multiplication and their blends to improve speed as well as reduce power consumption. The findings of few such studies are presented below.

This paper presented the design methods and Field Programmable Gate Array (FPGA) implementation of matrix multiplier in image and signal processing applications. This paper gives the detailed review of matrix product

implementation on FPGA where area, energy, speed, power dissipation, latency and time efficient methods are compared for different Xilinx families. Here also presented parallel architecture and parameterized system for matrix product used in FPGA. In this way, this literature will help in making performance characterization to implement high performance matrix multiplier on FPGA. [1]

Paper presented new algorithms and architectures for matrix multiplication on configurable devices. These have reduced energy dissipation and latency compared with the state-of-the-art field-programmable gate array (FPGA)-based designs. By profiling well-known designs, they identify "energy hot spots," which are responsible for most of the energy dissipation. Based on this, they develop algorithms and architectures that offer tradeoffs among the number of I/O ports, the number of registers, and the number of PEs. To avoid time-consuming low-level simulations for energy profiling and performance prediction of many alternate designs, they derived functions to represent the impact of algorithm design choices on the system-wide energy dissipation, area, and latency. These functions are used to either optimize the energy performance or provide tradeoffs for a family of candidate algorithms and architectures. For selected designs, they performed extensive low-level simulations using state-of-the-art tools and target FPGA devices. they show a design space for matrix multiplication on FPGAs that results in tradeoffs among energy, area, and latency. For example, their designs improve the energy performance of state-of-the-art FPGA-based designs by 29%–51%without any increase in the area–latency product. The latency of their designs is reduced one-third to one-fifteenth while area is increased 1.9–9.4 times. In terms of comprehensive metrics such as Energy-Area-Time, our designs exhibit superior performance compared with the state-of-the-art by 50%–79%.[4]

This paper present computations involving matrices form the kernel of a large spectrum of computationally demanding applications for which FPGAs have been utilized as accelerators. Their performances related to their underlying architectural and system parameters such as computational resources, memory and I/O bandwidth. A simple analytic model that gives an estimate of the performance of FPGA-based sparse matrix vector and matrix-matrix multiplication is presented, dense matrix multiplication being a special case. The efficiency of existing implementations are compared to the model and performance trends for future technologies examined. [6]

Paper presented 2x2 High-Speed matrix multiplier using Virtex 5 ML 507 Evaluation Platform (xc5vfx70t-1ff1136) FPGA. The hierarchical structuring has been used to optimize for multipliers using"Urdhava Trigyagbhyam" sutra (vertically and crosswise)which is one of the sutra for Vedic mathematics. Each element of matrix is represented by 16-bit.The coding has been done using VHDL and synthesized using Xilinx 13.2. A concept of design is hierarchical structuring; This gives less computation time for calculating the multiplication result. This also gives chances for modular design where smaller block can be used to design the bigger one. This will help in designing multiplier in VHDL, as its give effective utilization of structural method of modeling **.[7]**

Paper presented Matrix multiplication is the kernel operation used in many transform, image and discrete signal processing application. They developed new algorithms and new techniques for matrix multiplication on configurable devices. In this paper, they have proposed three designs for matrix-matrix multiplication. These design reduced hardware complexity, throughput rate and different input/output data format to match different application needs. These techniques have been designed implementation on Virtex-4 FPGA. They have synthesized the proposed designs and the existing design using Synopsys tools. Interestingly, the proposed parallel-fixed-input and multiple-output (PPI-MO) structure consumes 40% less energy than other two proposed structures and 70% less energy than the existing structure.[8]

Paper presented FPGA-based hardware realization of matrix multiplication based on distributed memory approach architecture. They propose an architecture that is capable of handling matrices of variable sizes our designs minimize the gate count, area, improvements in latency, computational time, and throughput for performing matrix multiplication and reduces the number of multiplication and additions hardware required to get the matrices multiplied on commercially available FPGA devices.[9]

III. SYSTEM ARCHITECTURE

The proposed work is aimed at finding high speed and low power consumption of matrix multiplication base on FPGA. Conventional method take more time for matrix multiplication calculation so we study different Vedic math's sutras for multiplication and use "Urdhva Triyagbhyam Algorithm" which take less timing.

3.1. conventional method for 3x3 matrix multiplication :

Two 3x3 matrix multiplies requires 27 multiplications and18 additions. Here, in 3x3 matrix multiplication, each bit is of 4-bit where 4-bitmultiplication and 8-bit addition is takes place. For32-bit adder uses 32 bitIP core (Intellectual Property).

Matrix A and Matrix B 3x3 matrices

$$A=\begin{pmatrix} a11 & a12 & a13 \\ a21 & a22 & a23 \\ a31 & a32 & a33 \end{pmatrix} \qquad B=\begin{pmatrix} b11 & b12 & b13 \\ b21 & b22 & b23 \\ b31 & b32 & b33 \end{pmatrix}$$

$$AXB=\begin{pmatrix} a11xb11+a12xb21+a13xb31 & a11xb12+a12xb22+a13xb32 & a11xb31+a12xb23+a13xb33 \\ a21xb11+a22xb21+a23xb31 & a21xb12+a22xb22+a23x32 & a21xb31+a22xb23+a23xb33 \\ a31xb11+a32x21+a33xb31 & a31xb12+a32xb22+a33xb32 & a31xb31+a32xb23+a33xb33 \end{pmatrix}$$

A X B = C

in this case 3x3 matrix multiplication each element in multiplication and addition takes place so it take more time for calculation time delay is occure.

3.2.0. Urdhva Triyagbhyam Algorithm:

The Sanskrit word 'Veda' means 'knowledge'. Vedic Mathematics is the name given to the ancient system of Indian Mathematics which was rediscovered from the Vedas between 1911 and 1918 by Sri Bharati KrsnaTirthaji (1884-1960). According to his research all of mathematics is based on sixteen Sutras, or word-formulae. Vedic Mathematics is much simpler and easy to understand than conventional mathematics .Urdhva Triyagbhyam is a multiplication Sutra(Algorithm) in Vedic Mathematics for the multiplication of decimal numbers. We used same idea to the binary numbers to make it compatible with the digital hardware. This is the general formula applicable to all cases of multiplication . Urdhva means Vertical and Triyagbhyam means Crosswise.

Steps:

a) Vertical Multiplication(LSB):

Multiply LSBs (Least Significant Bits) ‘1’ and ‘0’; placeproduct ‘0’ as LSB of the result.

b) Crosswise Multiplication:

Multiply Crosswise ‘1’ and ‘1’; ‘0’ and ‘1’; add the product terms and place obtained sum as middle term of the result.

c) Vertical Multiplication(MSB):

Multiply the MSBs (Most Significant Bits) ‘1’ and ‘1’; place product ‘1’ as MSB of the result:

Example : a1 a0 * b1 b0

Explanation for 2-bit Multiplication: a1 a0 * a1 a0

a1 a0
X b1 b0
---
a1 X b1 ; a1 X b0 + a0 X b1 ; a0 X b0

Similarly multiplication can be done for any digital numbers using Urdhva Triyagbhyam algorithm of ancient Indian Vedic mathematics.

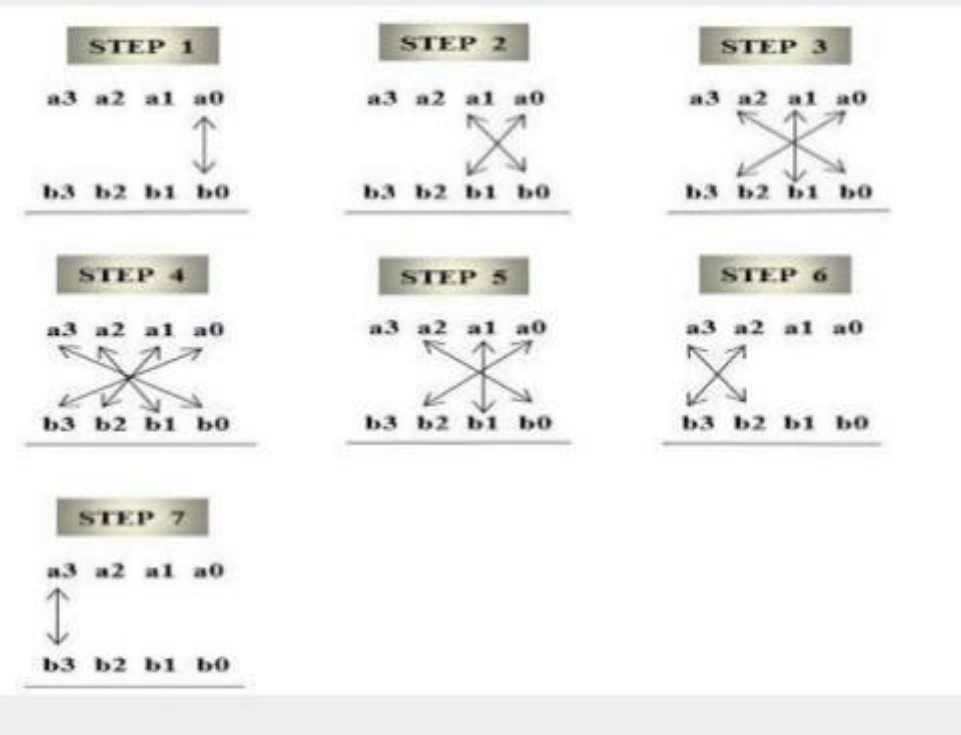
3.2.1. 4-bit multiplier:

The 4-bit multiplier is made by using 4, 2-bitmultiplier blocks and 3,4-bit adders. Here the multiplicands are of bit size (n=4) and the output is of bit size 8. As per the sutra ,the 4-bit (n) input is divided into small block of size n/2=2 which reduces the complexity. The newly formed block of 2 bits are given as input to 2-bit Vedic multiplier blocks. It will leads to high efficiency multiplier architecture. The output obtained from output of 2-bit Vedic multiplier block which is of 4 bits are given to the 4-bit adder. For 4-bit adder uses 4-bit IP core(Intellectual Property). The block diagram is shown in

a3 a2 | a1 a0 (4-bit multiplicand)

X b3 b2 | b1 b0 (4-bit multiplier)

P7 P6 P5 P4 P3 P2 P1 P0 (8-bit Result)



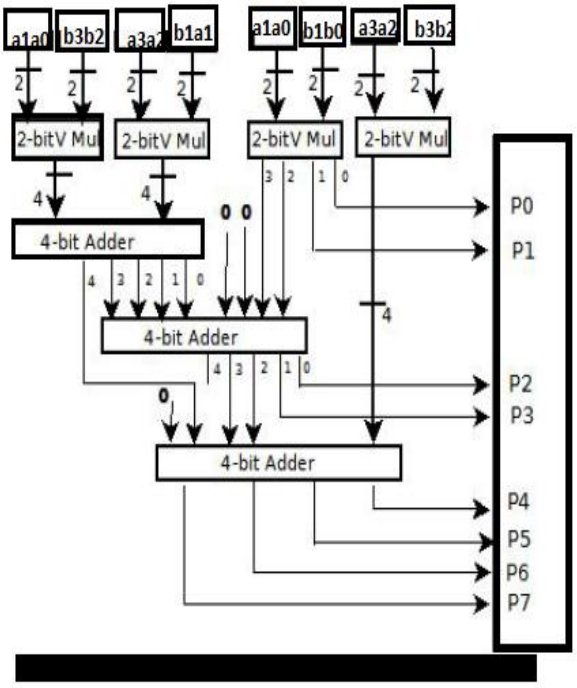


Figure1: 4 bit multiplier block

3.3. FPGA

A **field-programmable gate array** (**FPGA**) is an integrated circuit created to be configured by the customer after manufacturing—hence "field-programmable". The FPGA configuration is generally defined using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC) (circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare). FPGAs can be used to implement any logical function that an ASIC can perform. The ability to update the functionality after shipping, partial re-configuration of the portion of the design and the low non-recurring engineering costs relative to an ASIC design, offer advantages for many applications.

ADVANTAGES OF FPGA

FPGAs have become very popular in the recent years owing to the following advantages that they offer:

1) **Fast prototyping and turn-around time-**
2) **NRE cost is zero**
3) **High-Speed**
4) **Low cost**

3.4. VHDL

The **VHSIC Hardware Description Language** (VHDL) is a formal notation intended for use in all phases of the creation of electronic systems. Because it is both machine readable and human readable, it supports the development, verification, synthesis, and testing of hardware designs; the communication of hardware design data; and the maintenance, modification, and procurement of hardware

4.1. BENEFITS OF USING VHDL

- Executable specification
- Validate spec in system context (Subcontract)
- Functionality separated from implementation
- Simulate early and fast (Manage complexity)
- Explore design alternatives
- Get feedback (Produce better designs)
- Automatic synthesis and test generation (ATPG for ASICs)
- Increase productivity (Shorten time-to-market)
- Technology and tool independence (though FPGA features may be unexploited)
- Portable design data (Protect investment)

IV. Conclusion

Proposed work presents architecture for the multiplication of two matrices using Field Programmable Gate Array (FPGA).This paper presents unsigned two 3x3 High-Speed matrix multiplier The hierarchical structuring has been used to optimize for multipliers using “Urdhava Trigyagbhyam” sutra (vertically and crosswise)which is one of the sutra for Vedic mathematics. Each element of matrix is represented by 4-bit,output is of 8 bit. The coding has been done using VHDL and synthesized using Altera Quartus II. A concept of design is hierarchical structuring; This gives less computation time for calculating the multiplication result. We will synthesized the proposed designs and the existing design using Altera Quartus II tools**.**

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