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FPGA based Reconfigurable Digital Filter in Measurement System for Plasma Diagnostic

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Abstract*—*The raw signal acquired from plasma diagnostic contains useful information about plasma properties. The signal also contains unwanted noise. The signal is acquired in computer using digitizer and processed further with help of software to enhance the signal to noise ratio. Such offline software based processing is tedious and time consuming. The FPGA (Field programmable gate array) based signal processing with parameter tuning feature is reliable and efficient approach. The FPGA based reconfigurable digital filter is developed and checked with magnetic field measurement system and yields satisfactory results.

Keywords: *Plasma diagnostic, FPGA, digital filter, signal processing*

I. INTRODUCTION

The various plasma diagnostic [1] gives information about the plasma properties like temperature, density, time profile about plasma evolution, geometry about plasma, etc. The diagnostics are installed around Tokamak machine with different aim and configuration. Each diagnostic uses different sensors to sense the plasma. The sensors commonly used are avalanche photo diode, cameras operating in different wavelength, photo diode, thermocouple, photo multiplier tube, etc. The signal conditioning electronics is required for pulse shaping and amplification of incoming signal from sensor. The noise is inherent property of sensor which is again get deteriorated when it is coupled with SCE (Signal Conditioning Electronics). The cables associated with signal coupling at input and output of SCE also contributes to degradation of overall SNR (signal to noise ratio). The power supply converts the noisy mains supply to low level output which is used to power the SCE and sensor. The SCE output is transmitted to signal acquisition system for digitization and storage purpose. In general readily available digitizers are used for signal acquisition purpose. The computer with LabVIEW (National Instrument) software is incorporated for interfacing of digitizers, data acquisition and storage. The stored data is analyzed and processed to achieve desired SNR and sent to main server for processing purpose to extract useful information.

The software based signal processing on computer requires dedicated operator with system specific knowledge and software skill. The FPGA based signal processing [2] is efficient and with help of parameter tuning feature it is adaptive to any diagnostic configuration. The implementation of digital filter on FPGA offers many advantageous over digital signal processor (DSP) like parallel processing, high speed, reconfiguration, flexibility and low cost. In signal processing task such as filtering the incoming signal; the reconfiguration of various parameter of filters like type of filter, cut-off frequency, gain, order, etc. is required to change in run-time environment. In general the FPGA is intended to implement one static digital circuit which will not change in run time. To change the various parameters of filter; there are many techniques available. The parameter can be stored on internal memory of FPGA and it can be accessed as needed. The parameter and configuration data can be stored on computer memory and uploaded to FPGA as needed. In general the filter co-efficient to realize various filters and reference input waveforms to test the response of filterare obtained from LabVIEW or MATLAB software. There are two types of digital filter; finite impulse response (FIR) filter and infinite impulse response (IIR) filter [3, 4, 5, 6]. The linear phase response is easily obtained from FIR response while the IIR response is easy to implement for various dynamic characteristic of filter with less utilization of resources. In this document we are discussing the IIR filter implementation on FPGA for magnetic field measurement system

II. PROTOTYPE SETUP FOR SIGNAL MEASUREMENT

For few proto-type diagnostic; the readymade digitizer option is costly and so the digital oscilloscope based signal acquisition system is used. The LabVIEW software is used to communicate with oscilloscope and acquires the signal on computer. The four channel oscilloscope (DPO3054, Tektronix) is used as a signal acquisition device. The universal serial bus (USB) based communication is used to transfer the data from oscilloscope to computer offline. The magnetic field measurement set-up is developed for proto-type diagnostic. The gauss-meter instrument (F. W. BELL) gives analog signal output proportional to generated input magnetic field. The set-up for magnetic field measurement is shown in Fig. 1.

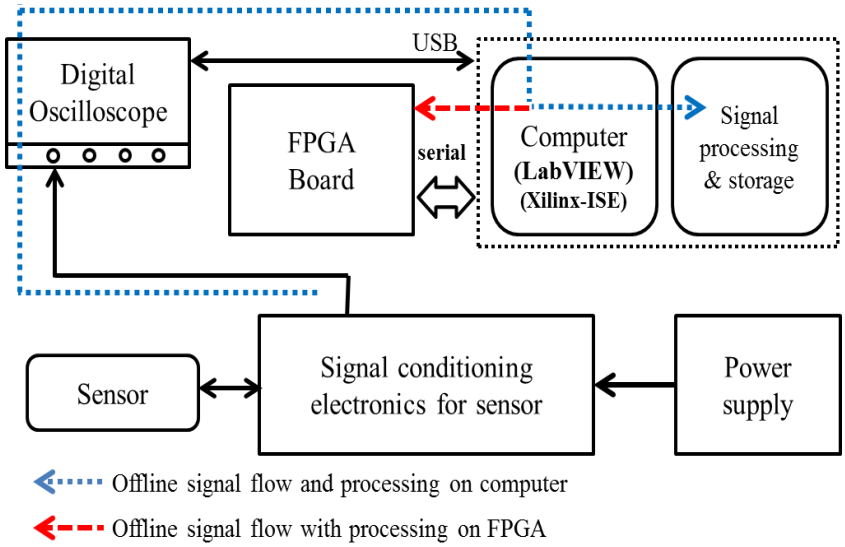

Figure 1: Signal flow diagram in prototype diagnostic setup

The figure shows the general setup for measuring signal from sensor in any plasma diagnostic setup. In magnetic field measurement the sensor used is hall probe sensor and it measures the magnetic field in axial direction. The signal conditioning electronics of the gauss-meter gives the analog voltage proportional to input magnetic field. The signal is acquired with desired sampling rate and dynamic range of internal ADC of oscilloscope. The LabVIEW based graphical user interface (GUI) is developed to communicate with oscilloscope.

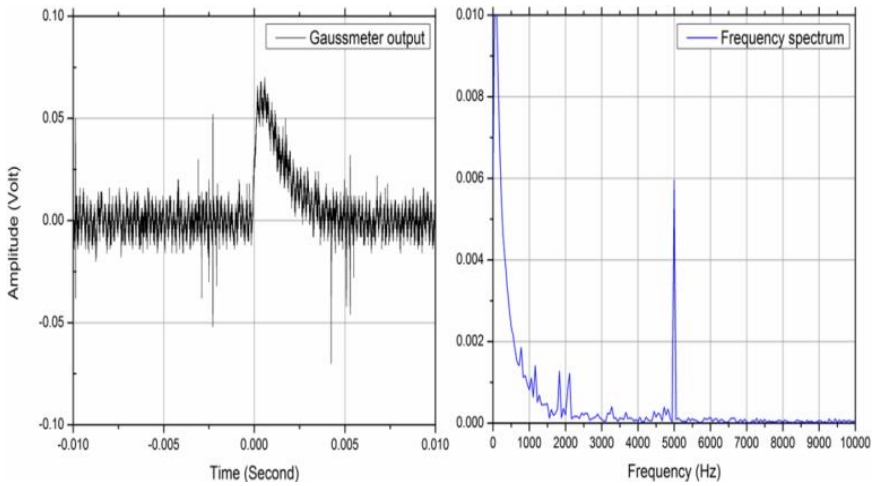

Figure 2: Acquired signal from oscilloscope and frequency spectrum

The acquired magnetic field data is stored on permanent storage of computer. The stored raw signal from gauss-meter is plotted as shown in Fig 2. The measured signal amplitude gives value of ~ 600 gauss of magnetic field. The acquired signal on oscilloscope is noisy with SNR of ~ 8.6 dB. The noise in signal gives error in measured magnetic field. The uncertainty in measured magnetic field due to input noise can be minimized with improvement of SNR. The variety of signal processing techniques is available to minimize noise. Appling filtering process on incoming signal is simple and efficient method to enhance SNR. To apply filter on signal, the knowledge about the frequency spectrum of incoming signal is required. The Origin software is used to extract frequency spectrum of incoming signal. The Fig 2 shows the spectrum of gauss-meter output. The low pass filter with cut-off frequency greater than 500 Hz is sufficient to attenuation of noise from acquired signal.

III. SIGNAL PROCESSING ON HARDWARE

There are two approaches for applying signal processing on incoming signals. In first approach, the pre-stored signal or acquired signal is processed offline with help of software on computer. The software based processing with LabVIEW is easily configurable with readily available library blocks. The signal processing block of library of LabVIEW is shown in Fig 3; the block is used with raw signal and filtered data at output stage is viewed on screen. In Fig3; the raw signals is acquired from gauss-meter and given to LabVIEW based digital IIR 4th order low pass Butterworth filter. The output filtered signal is shown in Fig 3; the effectiveness of filter is clearly visible.

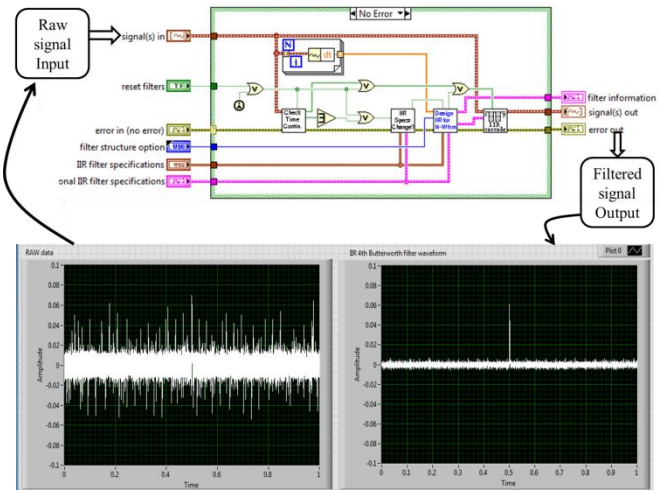

Figure 3: LabVIEW library blocks with input and output waveforms

The signal filtering process inside the LabVIEW with pre-stored data is able to execute in automated way. The whole process for acquiring data from oscilloscope and applying reconfigurable filter to acquired data for desired SNR integrated in one GUI. In software based signal processing approach; the system becomes computer dependent. In second approach of hardware based signal processing; the digital filter is implemented on FPGA processor. In this approach the system is independent from computer and the hardware is useful to accommodate in any real time control system. To develop hardware based filter, initially the FPGA board is used in offline mode where the pre-stored data is given to FPGA and the filtered data is extracted from FPGA to computer. The block diagram of hardware functionality is shown in Fig 4. The filter co-efficient and the raw signal are stored in FPGA internal memory. The parameter adjustment of realized filter like order of filter, cut-off frequency and types of filter is incorporated from external switch mounted on board. The filtered output data is monitored using chipscope tool. The raw signal and filter signal is plotted using Origin software for comparison.

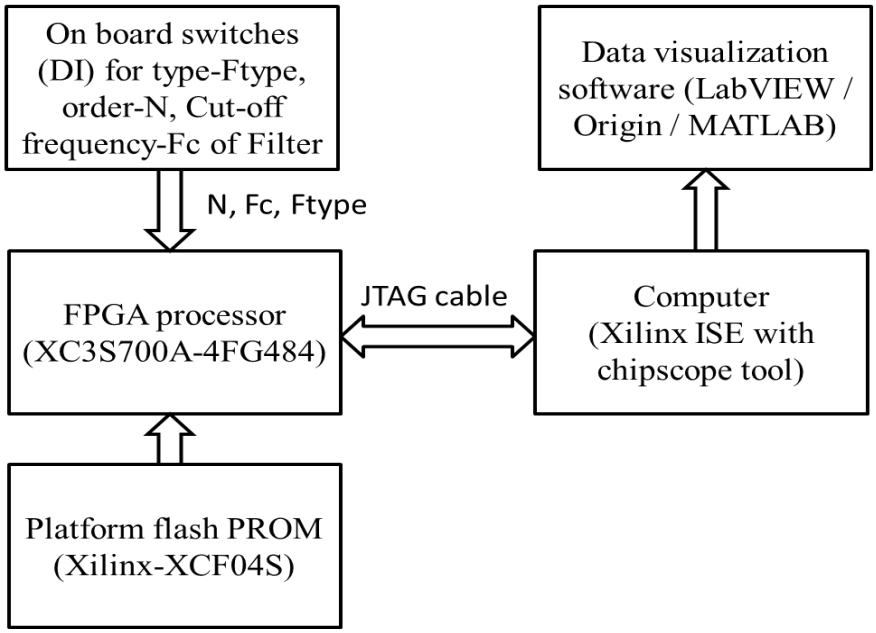

Figure 4: Hardware block diagram for FPGA based signal processing

There are two type of digital filter; (1) Finite impulse filter (FIR) (2) Infinite impulse filter (IIR). The transfer function of N tap FIR filter is given by;

$$H(z) = a_0 z^{-1} + a_2 z^{-2} + \cdots + a_{N-1} z^{-(N-1)} \qquad (1)$$


```
Assign I = type of filter (From external switches or digital input)
Assign j = enter low pass cut-off frequency (from external switches or digital input)
Assign k = number of order (minimum =2 , maximum = 8)
Filter:
Assign address of BROM = combination of (I, j, k)
Load coefficient from BROM to variables a1, a2, b0, b1, b2;
Assign x = input Raw data;
For i=0 to (no of samples) do
Sum_1[i] = x[i] * b0 + x[i-1] * b1 + x[i-2] * b2;
Sum_2 [i] = a1* y[i-1] + a2 * y[i-2];
Y[i] = sum_1[i] – sum_2[i];
If (clk) then
X[i-2] =x[i-1];
X[i-1]=x[i];
Y[i-1]= y[i];
Y[i-2] = y[i-1];
End if
End for
Cascade second order section (SOS) for N > 2 order with increment in k
GOTO Filter
Output = Y[i]
```

Figure 5: Pseudo code for designed reconfigurable filter

The digital IIR filter includes methods which permit to convert the analog filter into its equivalent digital filter. Transfer function of IIR filter is given by;

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2} + \cdots + b_{N-1} z^{-(N-1)}}{1 + a_1 z^{-1} + a_2 z^{-2} + \cdots + a_{N-1} z^{-(N-1)}} \quad (2)$$

The IIR filter becomes unstable when cut-off frequency is greater than half of sampling frequency. The IIR filters are recursive filter with feed-forward and feedback path. The pseudo code for designed reconfigurable filter is shown in Fig 5. The flowchart is shown in Fig 6, it shows the overall flow about the hardware based signal processing. The IIR filter co-efficient are available from LabVIEW or MATLAB software. The filters parameters are stored on internal memory of FPGA. The filter parameters can be stored on permanent memory of computer to reduce memory usage of FPGA. The filter types, cut-off frequency, order of filter, etc. are decided by observing at frequency spectrum of acquired raw signal. The Verilog software is used for writing program of filter in ISE software. The ISIM tool is used for software simulation while the chipscope tool is used to verify the on-board functionality of program.

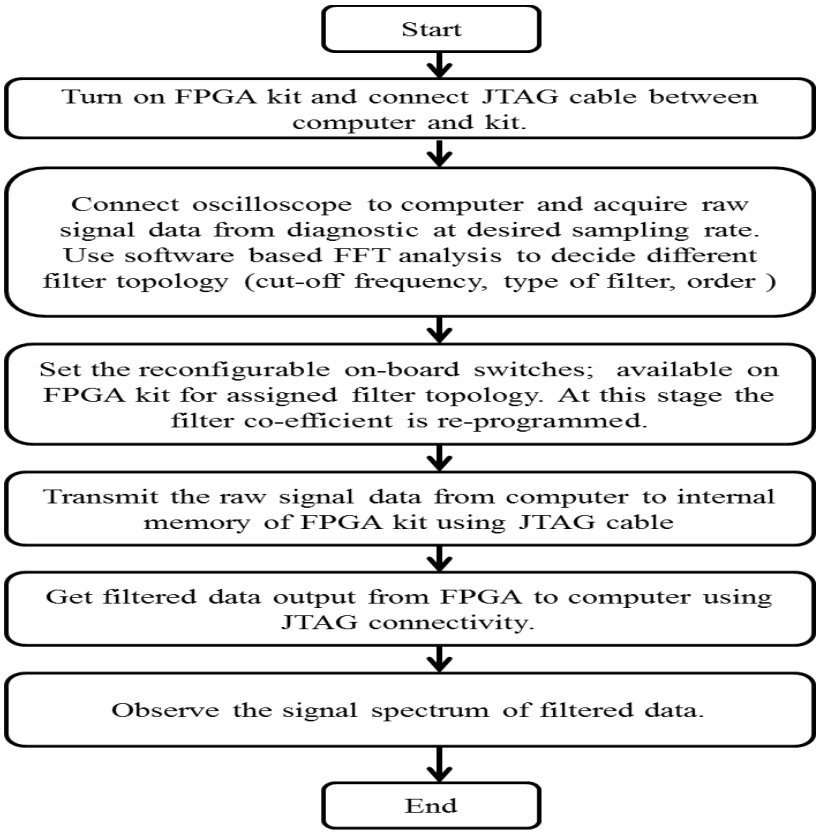

Figure 6: Flowchart for execution of hardware based digital filtering

The different topology and types of filter with different cut-off frequency and order is selected from available on-board switches. The second order filter is used recursively for higher order filter. The filter co-efficient and input data are stored in block RAM of FPGA using readily available IP core of ISE software. Three type of filter; Butterworth filter, Chebyshev type-I filter and elliptical filters are implemented on Spartan-3 processor.. The architecture of top module is shown in Fig 7. The input data for filter is of 8 bit; the filter is also tested for 12 bit and 16 bit input data. In first SOS (second order section) module which works as second order low pass filter; the input and output data are delayed and multiplied with pre-stored co-efficient (Order N = 2 in equation-2) to obtain filtered data. The second order module is connected in series to form higher order filter. In Fig 7 two SOS modules are used to form fourth order filter. The co-efficient data are of 8-bit fixed point.

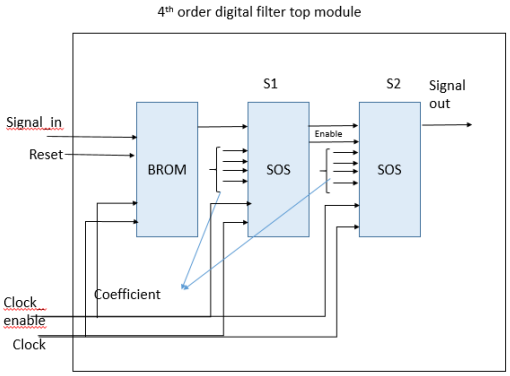

Figure 7: digital IIR filter top module

IV. RESULTS

The simulation results for the filter are shown in Fig 8. The latency for one SOS module is of 3 clock cycle.

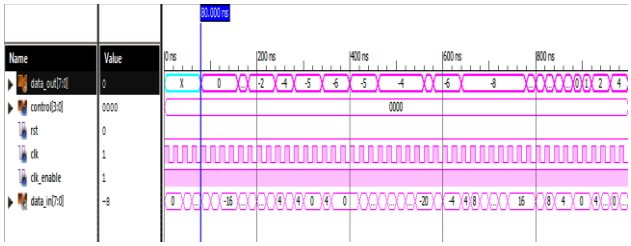

Figure 8: Simulation graph for filter

The enhancement in SNR with Butterworth filter having cut-off frequency of 2 KHz and different order is summarized in Table-1. The tables show that SNR is improving with help of digital filtering.

Table 1: Butterworth filter performance

Input SNR	Sampling frequency	Butterworth filter		
		Order	Cut-off	SNR
8.6 dB	100 KHz	2	2 KHz	12.1 dB
8.6 dB	100 KHz	4	2 KHz	12.7 dB
8.6 dB	100 KHz	6	2 KHz	12.4 dB
8.6 dB	100 KHz	8	2 KHz	12.1 dB

At higher order (N = 6, 8) the attenuation of output signal (lower output SNR) is observed due to changes in slope of transition band of filter. The cut-off frequency can be adjusted to maintain SNR at optimum level. The filtered output waveform is shown in Fig 9. The attenuation at greater than 2 KHz is observed on output spectrum of filtered signal. The improved SNR gives more reliable measurement of magnetic field particularly at low level of magnetic field where noise level is higher. The LabVIEW based filtered output is compared with the FPGA based filtered output data and found equivalent result. The SNR value of 12.4 dB is obtained with LabVIEW based 4th order IIR Butterworth filter. The elliptical filter is also implemented and compared with Butterworth filter at different cut-off frequency. For cut-off frequency of 500 Hz the elliptical filter gives SNR of 10.39 dB while for same configuration the Butterworth filter gives SNR of 10.6 dB.

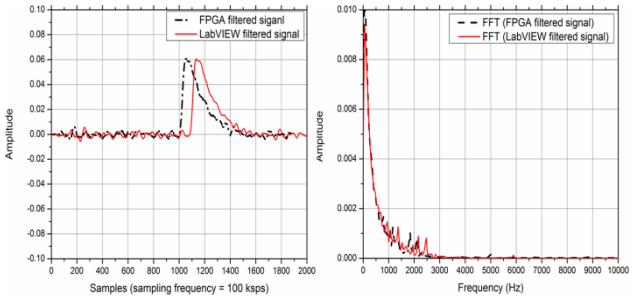

Figure 9: filter output waveform (N = 4, Fc = 2 KHz, Butterworth low pass filter)

The FPGA utilization summary for fourth order low pass Butterworth filter is show in table 2. The Spartan-3 series FPGA XC3S700A/AN processor is used for this work.

Table 2: FPGA utilization summary

Hardware utilization	Used	Available	utilized
Number of Slice	190	5888	3%
Number of slice flip flops	160	11776	2%
Number of 4 input LUTs	262	11776	2%
Number of Bounded IOBs	11	372	4%
Number of MULT18X18SIOs	12	20	60%
BRAM	1	20	5%

V. SUMMARY

The result shows effectiveness of FPGA as digital filter for enhancing SNR; which improves the reliability of signal measurement. The option to reconfigure the various parameter of filter is useful to adopt the same hardware for many different diagnostic. The FPGA processor with integrated ADC, DAC and LabVIEW interfacing offers many advantages for online signal processing and control application.

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