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Comparative analyis and study between 180nm and 90nm

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Abstract — *Leakage components are very important for estimation and reduction of leakage power especially in sub micron regimes in which threshold voltage, gate oxide thickness and channel length scale downwards. In present era it provides motivation to design a low power SRAM. This paper presents comparative analysis and study in both 180nm and 90nm, from which one can indentify that how the leakage issues become severe if technology node go downwards.*

Keywords- *low leakage memory design, SRAM, gate leakage current, subthreshold leakage current*

I. INTRODUCTION

Semiconductor memories are one of the most important subsystem of modern digital systems. A memory is a storage unit. In previous years many hardware devices like magnetic tapes, drives and optical disks were used. Random access memory (RAM) is widely used in all the devices for storage. In RAM, especially this paper concerns with the SRAM. In SRAM three modes are performed: read mode, write mode and standby mode. Here data is lost when power is removed means it is the volatile memory, but data does not “leak away” as like in a DRAM, so no need of refresh cycle in SRAM. Scaling of this technology has going on so large amount of memory can be fabricated on a single chip and due to that memories can able to do the operation speedy. Because of high density of chip, power dissipation increases. So the need for low power memory arises. For low power operation unnecessary usage of power should be reduced and one of the most important parameter for that is the leakage current.

II. CONVENTIONAL 6T SRAM

As shown in figure.1 this cell built up of two cross coupled inverters and two access transistors, connecting the cell to the bit lines. The access transistors are used to communicate with outside and cross coupled inverters makes the storage element. The cell is symmetrical and fully compatible with CMOS processes. Mainly three modes of SRAM are: read mode, write mode and standby mode.

2.1 Read cycle

In read cycle the stored content in the cross coupled inverter can be red. Suppose that memory content is „1“ and precharging both the bit lines at 1. Now assert the WL, which enables both the access transistors M5 and M6. Values of Q_bar and Q transferred to BL and BL_bar respectively. BL precharged and BL_bar discharge through M5 and M1 transistors to 0, here M1 is on because Q is 1. On BL side M4 is on because Q_bar is 0, it will try to pull up BL to VDD. If the memory content is „0“ then the operation perform is vice versa. The difference of BL and BL_bar should minimum and it is called delta, which will sense by a sense amplifier. Here the sensitivity is more than the read speed will be more.

2.2 Write Cycle

Write cycle starts by applying value we wish to write to the bit lines. If we wish to write 0 then apply 0 to the BL and 1 to the BL_bar. If we wish to write 1 then the values applied to bit lines should be reversed. Then WL asserted and value to be stored is latch in. Note that the reason this works is that the bit line input drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters. Careful sizing of the transistors in an SRAM cell is needed to ensure proper operation.

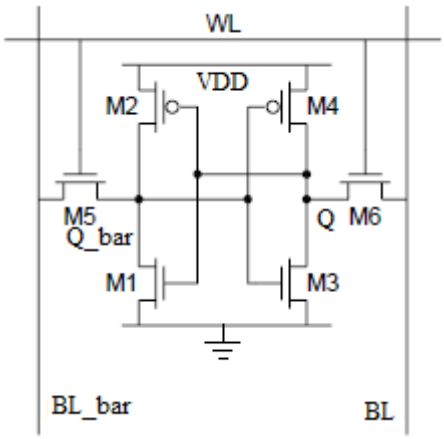


Fig. 1: 6T SRAM

2.3 Standby mode

If the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross-coupled inverters formed by M1-M4 will continue to reinforce each other as long as they are connected to the supply. In this mode no action could be taken and for retain the data the more power is consumed by SRAM, so the techniques are suggested to reduce the power consumption by reduction in leakage current.

III. LEAKAGE POWER COMPONENTS

In SRAM conventionally two components are prime those are: dynamic power dissipation and static power dissipation. Dynamic power dissipation is occurs because of charging and discharging of load capacitance and nonzero rise and fall time of input waveforms. Leakage power contains mainly three components.

3.1 Gate leakage

The current flowing into the gate of the transistor is also called tunneling. It results when tunneling of electrons, holes from the bulk silicon into the gate in an NMOS, PMOS respectively. It composed of major three components:

1. Gate to source and gate to drain overlap current.
2. Gate to channel currents.
3. Gate to substrate current.

Gate leakage is shown in fig.2

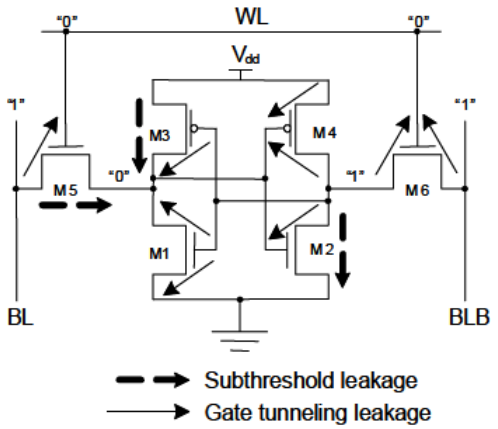


Fig. 2: Gate and subthreshold leakage current in 6T SRAM [1]

3.2 Subthreshold leakage

It happens when the transistor is operating in weak inversion region. It is the drain source current of a transistor when the gate source voltage (Vgs) is less than the threshold voltage. The subthreshold current depends on threshold voltage exponentially, which results in large subthreshold current especially short channel devices. In fig. 2 subthreshold leakage current is shown by the dotted arrow.

3.3 Junction tunnelling leakage

This is mainly a reverse biased pn junction leakage, which has mainly two components:
1.Minority carrier diffusion near the edge of depletion region.
2.Electron hole pair generation in depletion region of reverse biased junction.

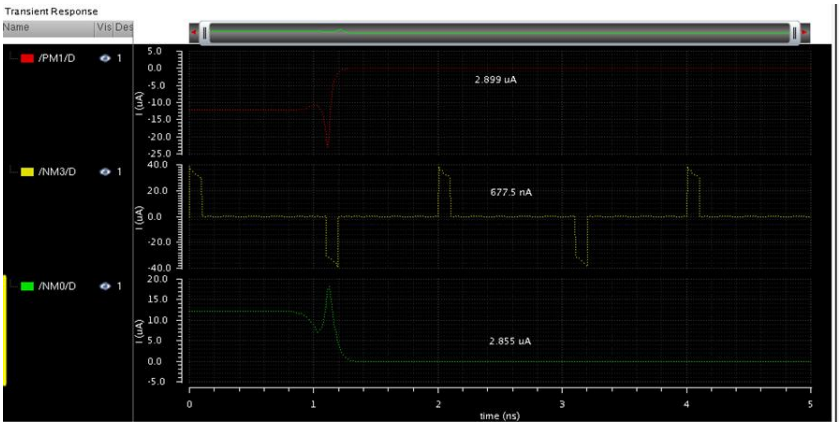
The junction tunneling current is an exponential function of reverse bias voltage across the junction and junction doping. This component is a negligible contributor to the total leakage current.

IV. SIMULATION RESULTS

4.1 Conventional SRAM in 180nm technology

4..1.1 Results of gate leakage currents

4.1.2 Results of subthreshold leakage current

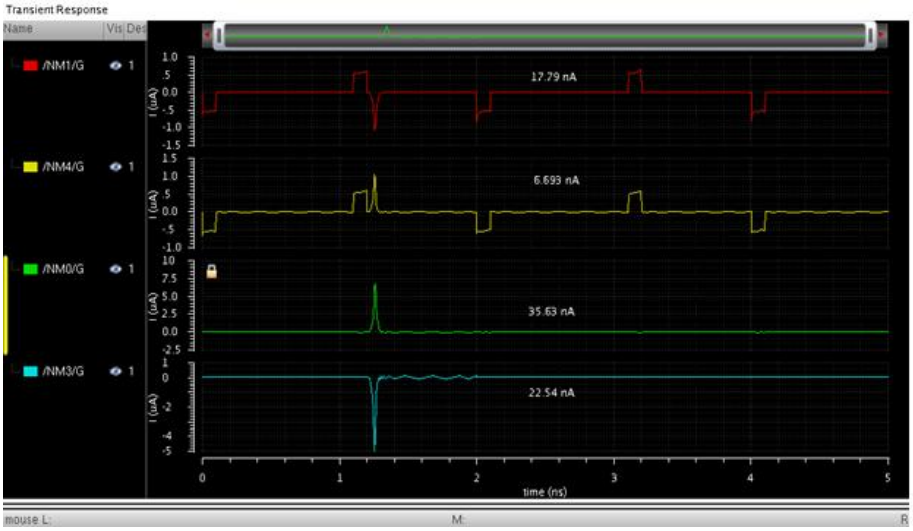


Total gate leakage current	**1.317uA**
Total subthreshold leakage current	**6.4315uA**
Total leakage current	**7.7485uA**

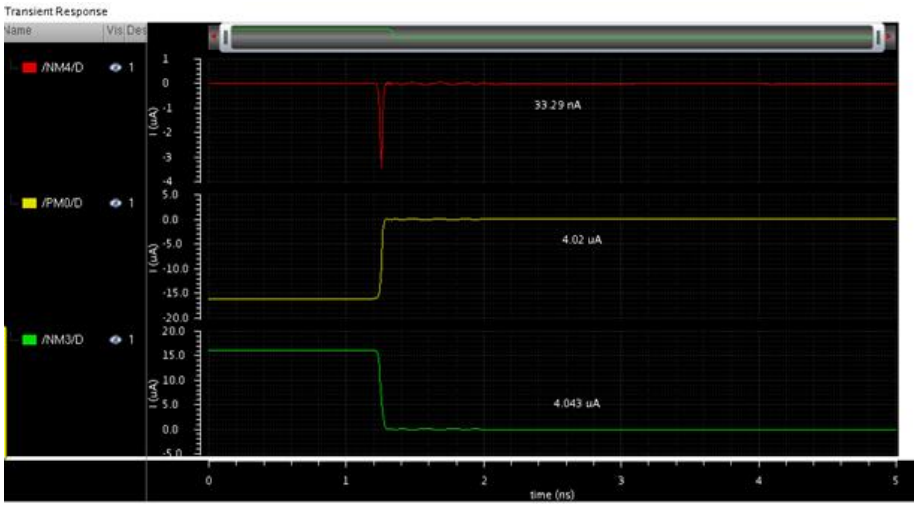
Table:1 Results for 180nm

4.2 Conventional SRAM in 90nm technology

4.2.1 Results of gate leakage currents



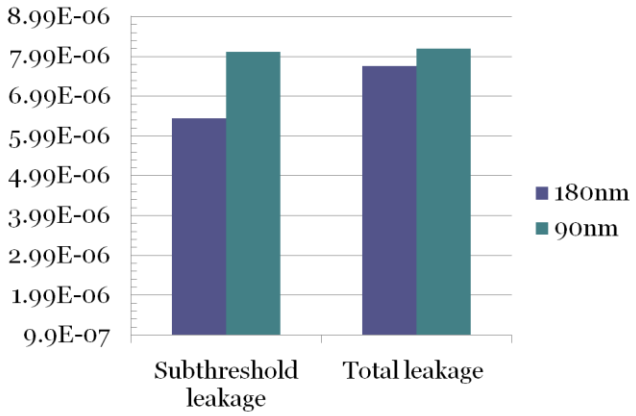
4.2.2 Results of subthreshold leakage current



Total gate leakage current (A)	**8.2653×10^{-8}**
Total subthreshold leakage current (A)	**8.096×10^{-6}**
Total leakage current	**8.178 uA**

Table:2 Results for 90nm

4.3 Technology comparison:



Graph 1: Comparison

V. CONCLUSION

From the simulation results which are perform on CADENCE tool and the graph it is clearly identify the leakage issues when the technology node go downwards. The main parameters which are considered before designing are the leakage parameter, performance in terms of speed, read delay, write delay, transition overhead and stability. Still it is the tread-off between parameters in designing of SRAM. So before choosing of any technique checking is very important in all aspects then selects the best appropriate technique which is most suitable to our application. For any technology node the analysis is very useful.

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